A 2.1µm High Dynamic Range CMOS Image Sensor with Sub-pixel and Lateral Overflow Integration Capacitor Architecture

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***Abstract*— This is a report on an Automotive CMOS image sensor using a pixel architecture of 2.1µm Sub-pixel and Lateral Overflow Integration Capacitor (LOFIC) readout, which consists of a large and small PD with intra-pixel capacitance. This sensor has a pixel pitch of 2.1 µm and is equipped with a Sub-Pixel with two photodiodes, one large and one small, and a MOS capacitor Floating Capacitor (FC) and a MOM capacitor Extra Capacitor (EC) in the pixel, and by connecting four signals in a single exposure, it has both a High Dynamic Range (HDR) of 105 dB and LED Flicker Mitigation (LFM), Motion artifact free.**

Keywords—CMOS Image Sensor, Automotive, HDR, LFM, Motion Artifact Free, Sub-pixel, LOFIC.

I. INTRODUCTION

In recent years, the performance of Automotive CMOS image sensor has become important for the advanced safety technologies. Dynamic range is key parameter for environment recognition, and it is required to capture image from dark to bright environment. In addition, pixel miniaturizations and noise reduction in high temperature are also important for improving recognition accuracy. And it is necessary to have LED flicker-free to recognize traffic lights.

A conventional HDR technology using the multi-exposure method [1–2] causes motion artifacts of moving object due to the sampling time difference. In addition, a motion artifact free technology using a Sub-pixel architecture with single-exposure method [3] causes to degradation of signal-to-noise ratio (SNR) at the composite boundary between large photodiodes and small photodiodes signals. To improve the SNR drop, its method to use two signals with a small photodiode [4-5]. However, it is not suitable with the pixel miniaturization because of the area efficiency is deteriorated by the addition of the transfer gate for small photodiodes.

We have developed a new sensor to address these issues. The characteristic of this sensor is that it has combined to LOFIC technology and Sub-pixel architecture without transfer gate for small photodiodes.

II. SENSOR ARCHITECTURE

A. Sensor Configuration

Figure 1 shows the block diagram of the CMOS image sensor. The pixel chip is fabricated by using a 90nm process for FEOL and 65nm process for BEOL. Read-out circuits (load MOS transistors, column ADCs, DAC), driver circuits (row drivers, row decoders), image signal processor, and other circuits (PLL, MIPI I/F, CPU, etc.) are all mounted to the logic chip using a 40 nm process.

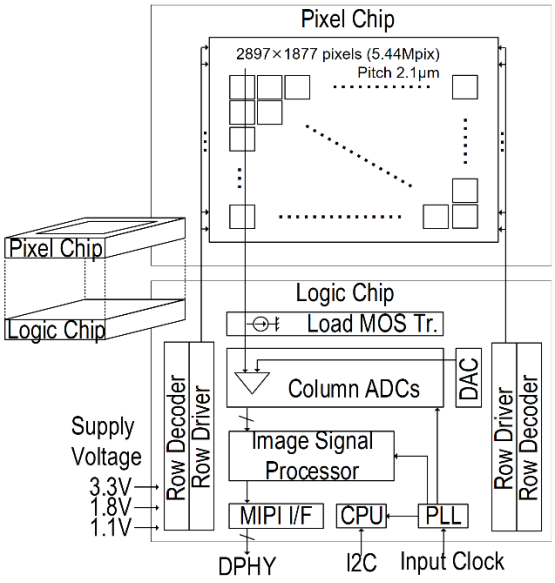

Figure 1. Sensor block diagram

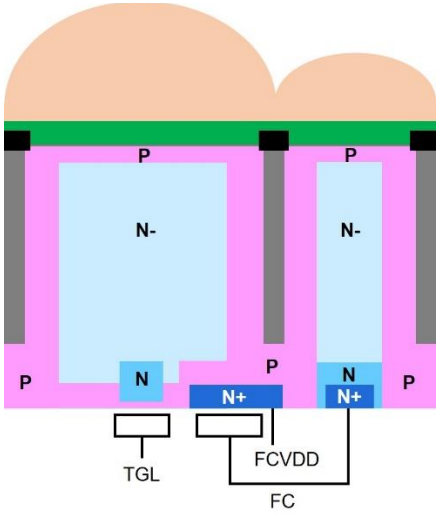

Figure 2. Cross-Section of a Sub-pixel

As shown in the Sub-pixel structure cross-sectional view of Figure 2, the high sensitivity photodiode (SP1) has a large on-chip micro lens (OCL), and the low sensitivity photodiode (SP2) has a small OCL. This makes the sensitivity ratio of SP1 to SP2 equal to 8.5:1. A Deep Trench Isolations (DTI) are employed in the silicon substrate to prevent optical crosstalk and the leakage of electrical charges from SP1 to SP2.

B. Pixel Circuit

Figure 3 shows the pixel schematic of the Sub-pixel and LOFIC architecture. This circuit employs a single large photodiode (SP1), a single small photodiode (SP2), a MOS capacitor Floating Capacitor (FC), a MOM capacitor Extra Capacitor (EC), three Floating Diffusions (FD) and six transistors. A total of three types of high-sensitivity, SP1 signals can be acquired: two types of signals acquired by switching conversion efficiency during the readout period, and a LOFIC signal acquired by storing the overflow charge from the photodiode in the EC capacitance during the exposure time. EC is connected to the FD2, and the supply voltage of the counter electrode is FHG. The low-sensitivity, SP2 signal is read out as a single signal in which the charge from the photodiode is accumulated in the FC capacitance. FC is connected to the FD3, and the supply voltage of the counter electrode is FCVDD.

Figure 4(a) and (b) shows the conventional and proposal SP2 cross-sectional view. As shown in Figure 4(a), the conventional SP2 has the TGS for transferring electron to FD. As shown in Figure 4(b), characteristics of a proposal SP2 structure is a direct-coupled technology in which ensures both the voltage amplitude of the FD and the transfer slope in the PD, maintains the transfer performance without TGS. This minimizes the occupancy of the SP2 area to 50% in a 2.1μm-pixel while suppressing dark current caused by the FD electric field and ensuring saturation charge without degradation.

In addition, for the EC capacitance that stores the overflowing charge from the photodiode in SP1, we established a method to form a second capacitance with a minimum process by forming the wiring layer in a comb-like shape to realize LOFIC drive as shown in Figure 5.

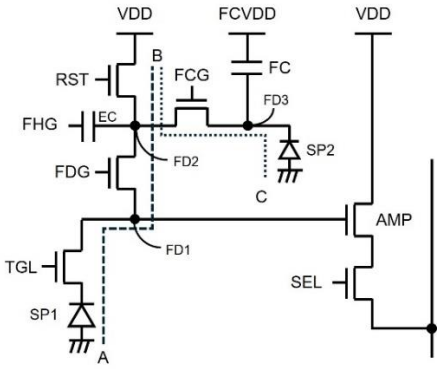

Figure 3. Pixel schematic

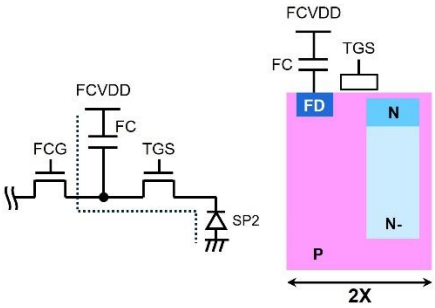

Figure 4(a). Conventional SP2 schematic and cross-sectional view of dotted line

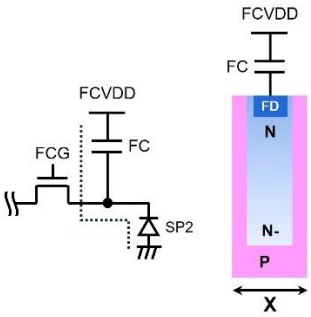

Figure 4(b). Proposal SP2 schematic and cross-sectional view of dotted line

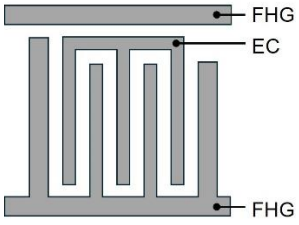

Figure 5. EC and FHG wiring design

C. Pixel Read-out Method

Figure 6 shows the pixel driving sequence. The signals that SP1 and SP2 are output serially. The electrical charges accumulated in SP1 are converted to a signal voltage in three modes, namely high conversion gain mode (SP1H), low conversion gain mode (SP1L) by switching FDG, and LOFIC mode (SP1EC) overflow charge from SP1 to EC

during the exposure time. The electrical charges accumulated in FC are read-out as SP2. In this manner, four signals are read out by one exposure. And the appropriate signal for each subject illumination is selected to acquire an HDR image.

Figure 7-8 shows a simplified potential diagram of SP1 and SP2 that considers the timing sequence in Figure 6. The cross section shows the path of the dotted line A-B and C-B in Figure 3. First, an exposure of SP1 and SP2 begins by the reset of SP1, SP2, EC and FC (a). During exposure time, FHG and FCVDD are continuously low voltage for reduce the FPN of SP1EC and SP2. In addition, all switching transistor is off (b). Then, SP1L reset level is sampled when FDG turned on (c) , and after that SP1H reset level is sampled when FDG is turned off (d). Subsequently, SP1H signal level is sampled after switching TGL (e), and SP1L signal level is sampled after switching TGL once again during FDG turned on (f). Therefore, both SP1H and SP1L can be read-out by performing Correlated Double Sampling (CDS) for each reset and signal level. Subsequently, SP1EC signal level is sampled at the same potential of SP1L signal level (g). After that, SP1EC reset level is sampled after RST is turned on (h). In these operations can read out all charge of the SP1 and EC as a LOFIC signal. Next, the signal that comes from SP2 is read, in which the signal level is sampled first during FCG is turned on (i), followed by the reset level after RST is turned on (k). Because the signal charges are accumulated in FC, it cannot be reset for sampling the signal level. SP1EC and SP2 are read out by performing Delta Reset Sampling (DRS). The drawback of DRS is that kTC noise cannot be removed. However, it can be suppressed by securing the capacitance of EC and FC sufficiently.

In addition, the FHG voltage of the electrode opposite the FD of the EC capacitance is made variable during the exposure time, so that the dark current and saturation charge of the EC storage area can be controlled. And the diffusion capacitance that stores the overflowing charge from SP1 required for LOFIC drive and the diffusion capacitance that stores the overflowing charge from SP2 required for Sub-Pixel are connected via the FCG transistor, the relationship between the off potential of the FCG transistor during the exposure time and the reset transistor's off. Therefore, it is important to set the relationship between the off potential of the FCG transistor and the off potential of the reset transistor during the exposure time appropriately.

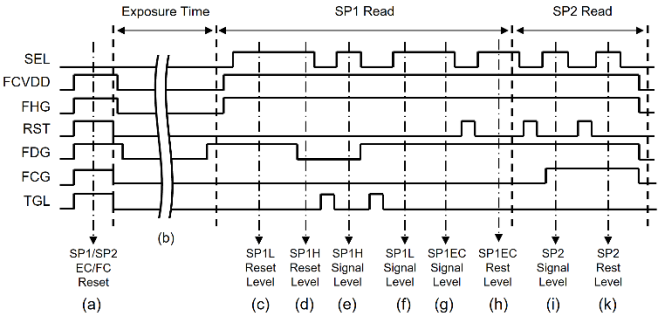

Figure 6. Timing Sequence

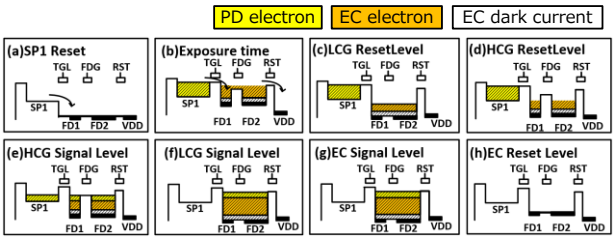

Figure 7. SP1 potential diagram (A-B in Fig.3)

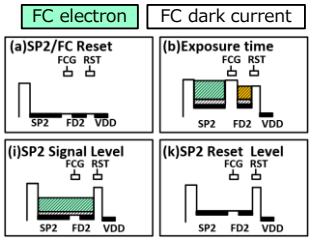

Figure 8. SP2 potential diagram (C-B in Fig.3)

III. SENSOR CHARACTERISTICS

A. *Sensor Characteristics*

Figure 9 shows the photo responses for SP1H, SP1L, SP1EC, and SP2. The linear Full Well Capacity(FWC) of SP1 is 16000 e-, SP1EC (LOFIC) is 50500 e- and SP2 is 58000 e- , respectively. Figure 10 shows the FHG voltage dependency of SP1L-SP1EC SNR drop and dynamic range of SP1. As the FHG voltage increases, dynamic range of SP1 is expanded due to increase the FD2 FWC. On the other hand, SNR drop is deterioration due to increase the FPN is caused by the variation of FD2 dark current. The SNR drop and dynamic range of SP1 have a trade-off relationship. Figure 11 shows the FCVDD voltage dependency of SP1EC-SP2 SNR drop and dynamic range of SP1-SP2. The FCVDD has the same relationship as the FHG. The optimum value of SNR drop and dynamic range can be derived by controlling the voltage of FHG and FCVDD. Figure 12 shows the SNR curve of the synthesized signals. It consists of four types of signals. These allowed us to significantly improve the connected SN by increasing the LOFIC signal by one more step between the SP1 photodiode signal and the SP2 signal, which is a feature of Sub-Pixel. We have successfully improved SNR drop by about 13dB with the Sub-pixel and LOFIC pixel architecture compared to using Sub-pixel alone. And improved Dynamic range by 20dB compared to using LOFIC drive alone in SP1.

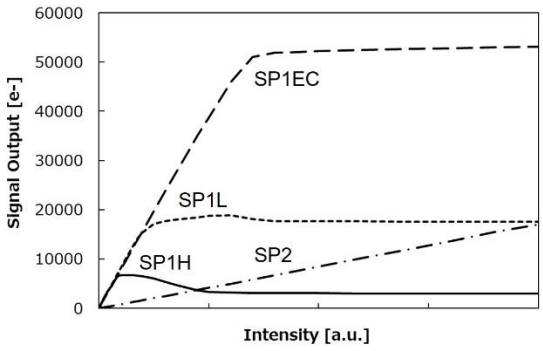

Figure 9. Photo response of SP1 and SP2

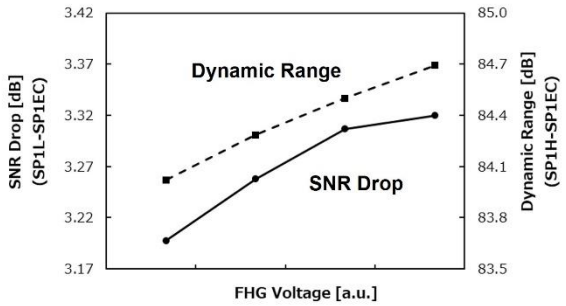

Figure 10. FHG dependency of SNR drop and Dynamic Range

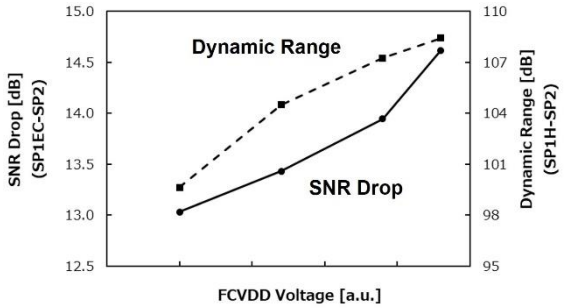

Figure 11. FCVDD dependency of SNR drop and Dynamic Range

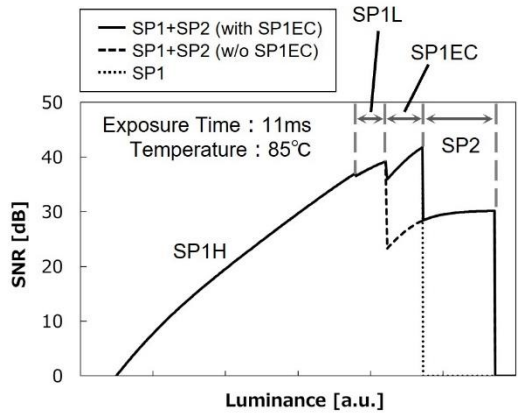

Figure 12. SNR curve

B. Synthesized Image

Figure 13 shows synthesized image of a high dynamic range scene at Tj = 85℃ with an exposure time of 11ms. Figure 13 (a) shows an image of composition signals with SP1H, SP1L and SP1EC. This image can be observed that the signals of highlight object are saturated.

Figure 13 (b) shows an image of composition signals with SP1H, SP1L, SP1EC and SP2. This image can be observed that the objects from dark to highlight are accurately captured, such as in the darkness of the tunnel and the Sun. And it can capture LED flicker free images due to long exposure time (11ms).

Figure 13(a). Capture image (SP1H + SP1L + SP1EC)

Figure 13(b). Capture image (SP1H + SP1L + SP1EC + SP2)

TABLE1 Pixel performance

		Unit	Large PD (SP1)	LOFIC (SP1EC)	Small PD (SP2)
Power Supply		V	3.3 / 1.8 / 1.1		
Process Technology		-	Pixel : FE90nm / BE65nm 4Cu Logic : 40nm 6Cu 1AL		
Pixel Pitch		μm	2.1		
Pixel Array		pixel	2897(H) x 1877(V) = 5.44M		
Color		-	Red, Green, Blue		
HDR Technology	In-pixel Capacitor	-	MOM		MOS
	Sensitivity Ratio	times	1.0		8.5
Random Noise @ RT		e- rms	1.4	46.4	59.6
Sensitivity (3200K with IR cutfilter)		e-/lx·s	13200		1900
Full-well Capacity		e-	16000	50500	58000
Dynamic Range (Single Exp.)		dB	105		

IV. CONCLUSIONS

TABLE1 shows pixel performance. We have developed a new CMOS image sensor that a combined LOFIC and Sub-pixel architecture with a pixel pitch of 2.1μm. It achieves both a high dynamic range of 105dB and SNR drop 28dB in a single exposure, further realizing LFM.

ACKNOWLEDGMENT

The authors would like to thank Y. Hattori, Y. Shirai, Y. Sugimori and T. Taura for their support and advice regarding the sensor design and evaluation. The authors also appreciate the support from the members of Sony Semiconductor Solutions Corp and Sony Semiconductor Manufacturing Corp.

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